

14-Channel Static TFT LCD Reference Voltage Generator with 1-Channel V_{COM}

The ISL24002 is a 14-Channel static reference voltage generator with a 1-Channel V_{COM} buffer.

The ISL24002 is available in 32 Ld thermal enhanced TQFN package. It is specified for operation over the -40°C to $+85^{\circ}\text{C}$ industrial temperature range.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE ($^{\circ}\text{C}$)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL24002IRTZ*	ISL240 02IRTZ	-40 to +85	32 LD TQFN	MDP0051

*Add "-T13" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

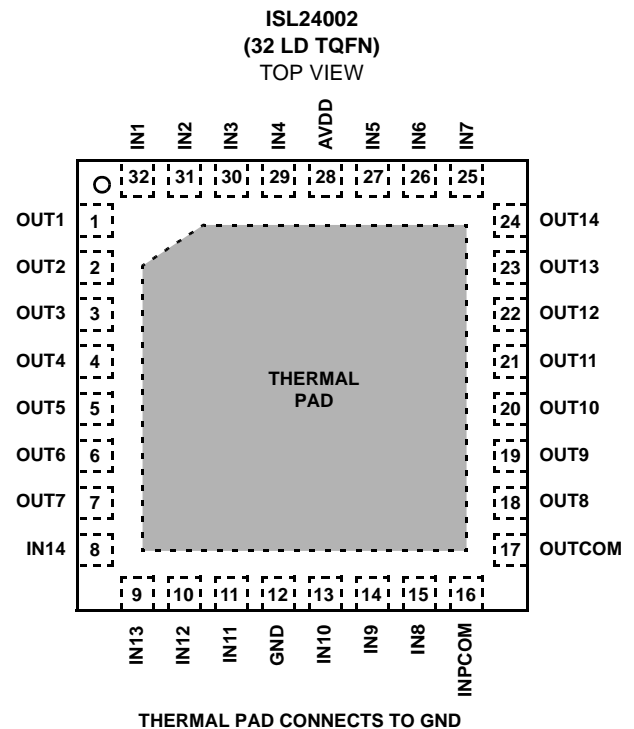
Features

- 18V Output Range
- Rail-to-Rail Input/Output Voltage Range
- 14-Input Channels
- 14-Output Channels Each with 30mA Peak Output Current
- 1-Channel V_{COM} with 100mA Peak Output Current
- 32 Ld TQFN Package
- Pb-Free (RoHS Compliant)

Applications

- TFT-LCD Panels

Pinout



Absolute Maximum Ratings (T_A = +25°C)

Driver Positive Supply Voltage Range (A _{VDD})+19V
Input Voltage Range-0.5V to A _{VDD} + 0.5V
Output Voltage Range-0.5V to A _{VDD} + 0.5V
IOUT (Channel Reference Buffers) 30mA
IOUT(V _{COM} Buffer) 100mA
ESD Rating	
Human Body Model3000V
Machine Model300V
Charged Device Model1500V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ _{JA} (°C/W)
32 Lead TQFN 34
Junction Temperature Range -40° to +135°C
Ambient Temperature Range -40° to +85°C
Storage Temperature Range -65°C to +150°C
Pb-free Reflow Profilesee link below
	http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.

Electrical Specifications A_{VDD} = 15V, T_A = +25°C, Unless Otherwise Specified.

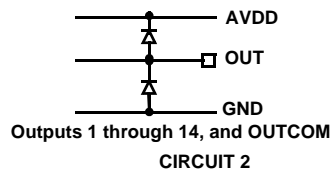
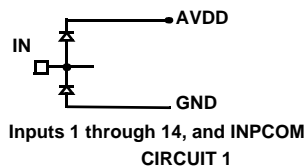
PARAMETER	DESCRIPTION	CONDITION	MIN (Note 2)	TYP	MAX (Note 2)	UNITS
REFERENCE BUFFER SECTION						
V _{OL}	Low Level Output Voltage	I _L = ±5mA		0.08	0.15	V
V _{OH}	High Level Output Voltage	I _L = ±5mA	14.82	14.92		V
V _{OS}	Input Offset Voltage	V _{IN} = 1.9V		2	15	mV
I _L	Input Leakage Current	V _{IN} = GMD, A _{VDD}		2	50	nA
SR	Slew Rate	Outputs 1 to 14, Measured 20% to 80%		4.5		V/μs
BW	-3dB Bandwidth	Output 1 to Output 14 R _L = 10kΩ, R _{OUT} = 0Ω, C _L = 10pF		5.5		MHz
I _{SC}	Short Circuit Current	Output 1 to Output 14		±200		mA
PSRR	Power Supply Rejection Ratio	V _{IN} = 1.9V, A _{VDD} = 10V, 15V		80		dB
OUTCOM AMPLIFIER SECTION						
V _{OL}	Low Level Output Voltage	I _L = ±5mA		0.05	0.15	V
V _{OH}	High Level Output Voltage	I _L = ±5mA	14.85	14.92		V
V _{OS}	Input Offset Voltage	V _{IN} = 1.9V		1	18	mV
I _L	Input Leakage Current	V _{IN} = GND, A _{VDD}		2	50	nA
SR	Slew Rate	OUTCOM, Measured 20% to 80%		40		V/μs
BW	-3dB Bandwidth	OUTCOM R _L = 10kΩ, R _{OUT} = 0Ω, C _L = 10pF		15		MHz
I _{SC}	Short Circuit Current	OUTCOM		±480		mA
PSRR	Power Supply Rejection Ratio	V _{IN} = 1.9V, A _{VDD} = 10V, 15V		80		dB
T _{TS}	Thermal Shutdown Temperature	Package temperature where the internal die will automatically shut down until it cools to below its maximum junction temperature.		140		°C
POWER SUPPLY SECTION						
Power Supply	Recommended Operating Voltage (A _{VDD})		5		18	V
I(A _{VDD})	Supply Current			10	15	mA

NOTES:

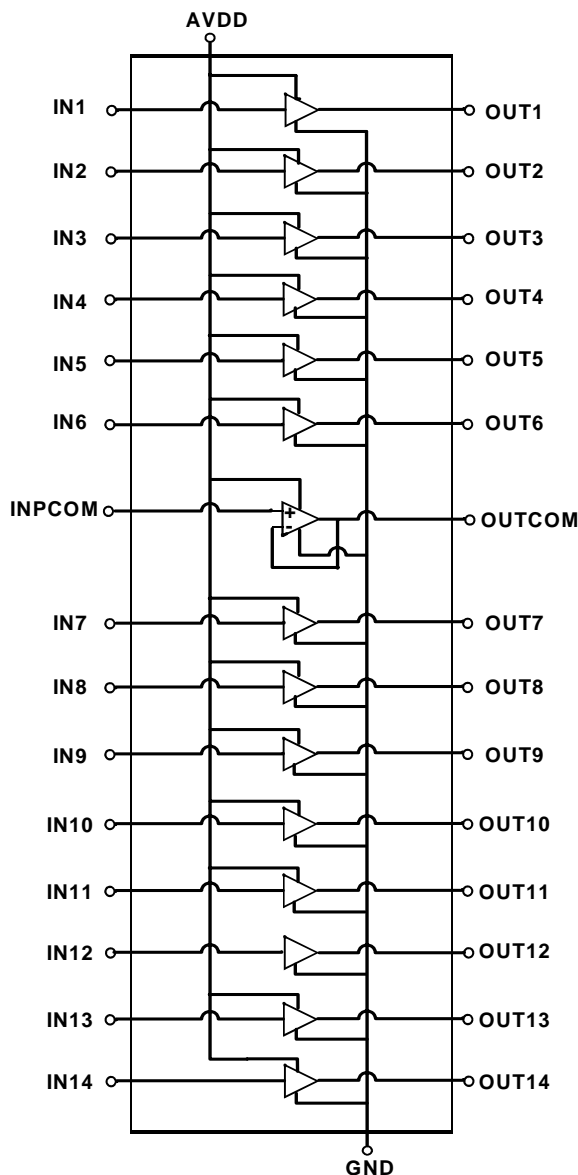
2. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Pin Descriptions

PIN NUMBER	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
1	OUT1	2	Analog Output 1
2	OUT2	2	Analog Output 2
3	OUT3	2	Analog Output 3
4	OUT4	2	Analog Output 4
5	OUT5	2	Analog Output 5
6	OUT6	2	Analog Output 6
7	OUT7	2	Analog Output 7
8	IN14	1	Analog Input 14
9	IN13	1	Analog Input 13
10	IN12	1	Analog Input 12
11	IN11	1	Analog Input 11
12	GND		Ground
13	IN10	1	Analog Input 10
14	IN9	1	Analog Input 9
15	IN8	1	Analog Input 8
16	INPCOM	1	Analog Input
17	OUTCOM	2	Analog Output
18	OUT8	2	Analog Output 8
19	OUT9	2	Analog Output 9
20	OUT10	2	Analog Output 10
21	OUT11	2	Analog Output 11
22	OUT12	2	Analog Output 12
23	OUT13	2	Analog Output 13
24	OUT14	2	Analog Output 14
25	IN7	1	Analog Input 7
26	IN6	1	Analog Input 6
27	IN5	1	Analog Input 5
28	AVDD		Analog Power
29	IN4	1	Analog Input 4
30	IN3	1	Analog Input 3
31	IN2	1	Analog Input 2
32	IN1	1	Analog Input 1



Functional Block Diagram



Application Information

Product Description

The ISL24002 is a 14-Channel static reference voltage generator with a 1-Channel V_{COM} buffer. Each input channel consists of a static voltage reference generator. All channel outputs are capable of swinging rail-to-rail. The V_{COM} buffer is capable of driving a large peak current into highly capacitive loads while ensuring a rail-to-rail voltage swing.

The ISL24002 is available in a 32 Ld thermal enhanced TQFN package. It is specified for operation over the -40°C to $+85^{\circ}\text{C}$ industrial temperature range.

Supply Voltage Range and Input Compatibility

The ISL24002 is designed for operation on supply voltages from 5V to 18V. Each channel input pin and INPCOM can be driven rail-to-rail.

Power Supply Bypassing and Printed Circuit Board Layout

Good printed circuit board layout is necessary for optimum performance. A low impedance and clean analog ground plane should be used for the ISL24002. The traces from the ground pin to the ground plane must be very short. The thermal pad should be connected to the analog ground plane. Trace length should be as short as possible and all power supply pins must be well bypassed.

Test Circuit

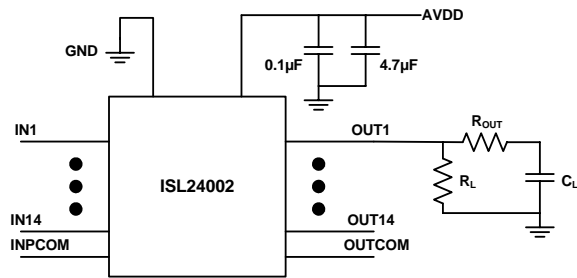


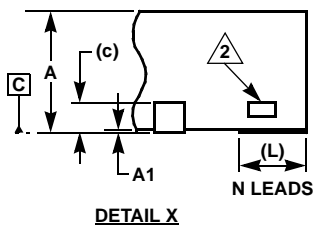
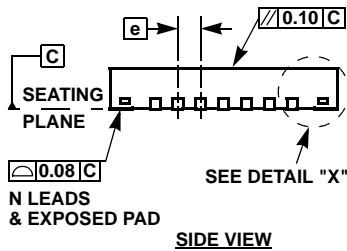
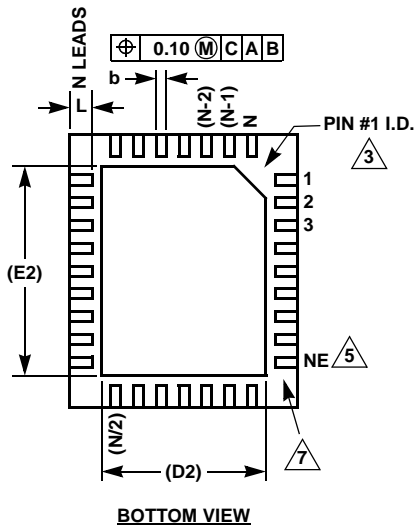
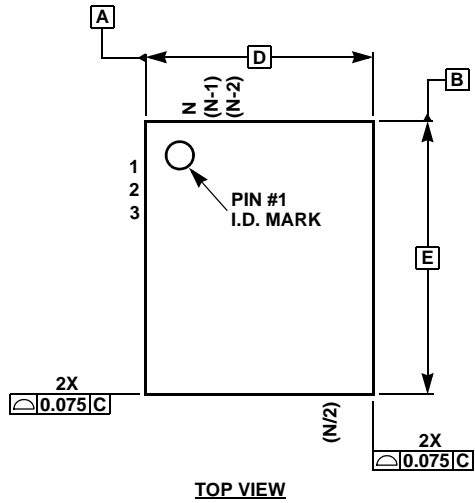
FIGURE 1. TEST CIRCUIT

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

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TQFN (Thin Quad Flat No-Lead) Package Family



MDP0051

TQFN (THIN QUAD FLAT NO-LEAD) PACKAGE FAMILY
(COMPLIANT TO JEDEC MO-220)

SYMBOL	MILLIMETERS		TOLERANCE	NOTES
	TQFN 28	TQFN 32		
A	0.75	0.75	±0.05	-
A1	0.02	0.02	+0.03/-0.02	-
b	0.325	0.25	±0.02	-
c	0.20	0.20	Reference	-
D	6.00	5.00	Basic	-
D2	4.70	3.10	Reference	8
E	6.00	5.00	Basic	-
E2	4.70	3.10	Reference	8
e	0.65	0.50	Basic	-
L	0.40	0.40	±0.05	-
N	28	32	Reference	4
ND	7	8	Reference	6
NE	7	8	Reference	5

Rev 1 2/07

NOTES:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Tiebar view shown is a non-functional feature.
3. Bottom-side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the "E" side of the package (or Y-direction).
6. ND is the number of terminals on the "D" side of the package (or X-direction). $ND = (N/2) - NE$.
7. Inward end of terminal may be square or circular in shape with radius $(b/2)$ as shown.
8. If two values are listed, multiple exposed pad options are available. Refer to device-specific datasheet.
9. Package outline drawing is generic.